优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

0755-83047638
ysbdt@szyoushang.cn
www.szyoushang.cn

企业微信二维码

企业QQ二维码

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max T_A = +25°C
30V	14mΩ @ V_{GS} = 10V	8.6A
	20mΩ @ V_{GS} = 4.5V	7.1A

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Backlighting
- Power Management Functions
- DC-DC Converters

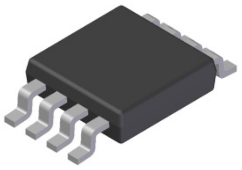
Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

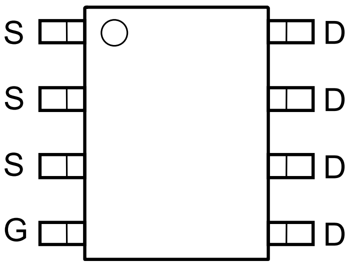
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.072g (approximate)

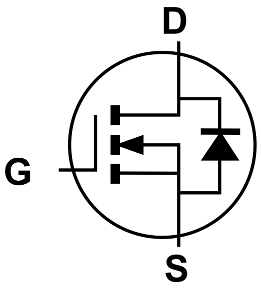
SO-8



Top View



Top View
Internal Schematic



Equivalent circuit

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±25	V
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +70°C	I_D	8.6 6.3	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	11.8 9.0	A
Maximum Body Diode Forward Current (Note 6)			I_S	2.4	A
Pulsed Drain Current (Note 7)			I_{DM}	50	A

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	1.46	W
	T_A = +70°C		0.9	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	86	°C/W
	t<10s		46	
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	1.7	W
	T_A = +70°C		1.0	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	75	°C/W
	t<10s		40	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	15	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	0.8	1.2	1.6	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	—	11 14	14 20	mΩ	V_{GS} = 10V, I_D = 9A V_{GS} = 4.5V, I_D = 7A
Forward Transconductance	g_{fs}	—	8	—	S	V_{DS} = 10V, I_D = 9A
Diode Forward Voltage (Note 8)	V_{SD}	—	0.72	0.94	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	798	—	pF	V_{DS} = 10V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	128	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	122	—	pF	
Gate Resistance	R_G	—	1.37	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge	Q_g	—	8.7	—	nC	V_{GS} = 5V, V_{DS} = 15V, I_D = 9A
Gate-Source Charge	Q_{gs}	—	1.7	—		
Gate-Drain Charge	Q_{gd}	—	2.4	—		
Turn-On Delay Time	$t_{d(on)}$	—	5.03	—	ns	V_{DD} = 15V, V_{GEN} = 10V, R_L = 15Ω, R_G = 6.0Ω, I_D = 1A
Rise Time	t_r	—	4.50	—		
Turn-Off Delay Time	$t_{d(off)}$	—	26.33	—		
Fall Time	t_f	—	8.55	—		

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout
7. Repetitive rating, pulse width limited by junction temperature.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

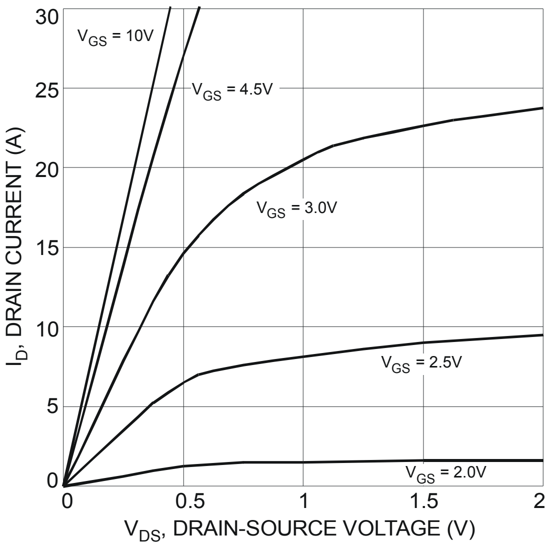


Fig. 1 Typical Output Characteristic

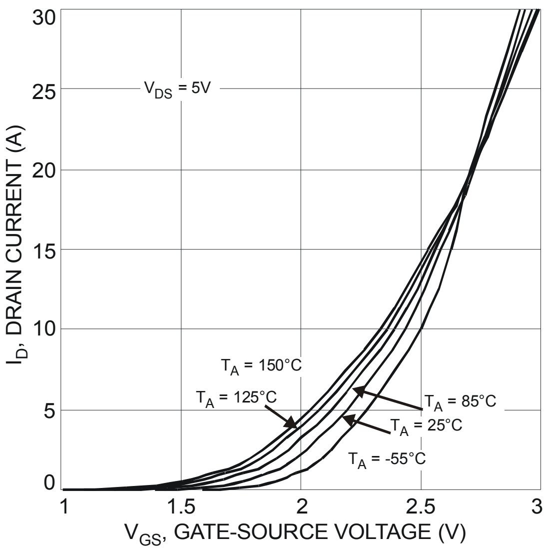


Fig. 2 Typical Transfer Characteristic

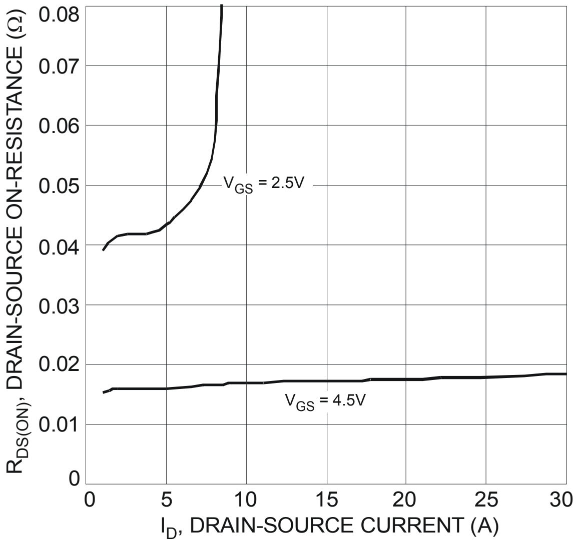


Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

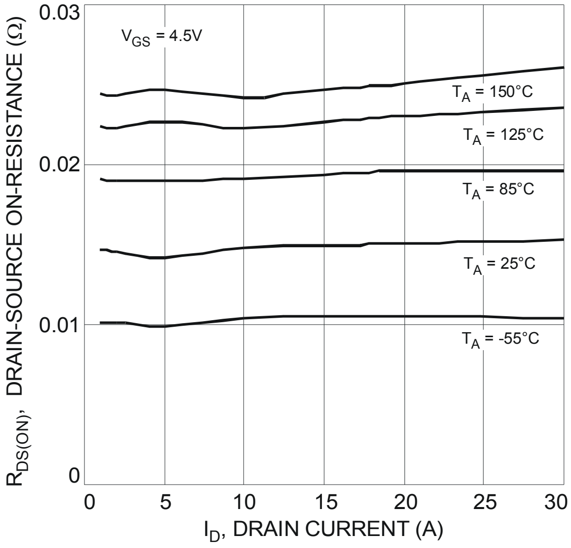


Fig. 4 Typical On-Resistance
vs. Drain Current and Temperature

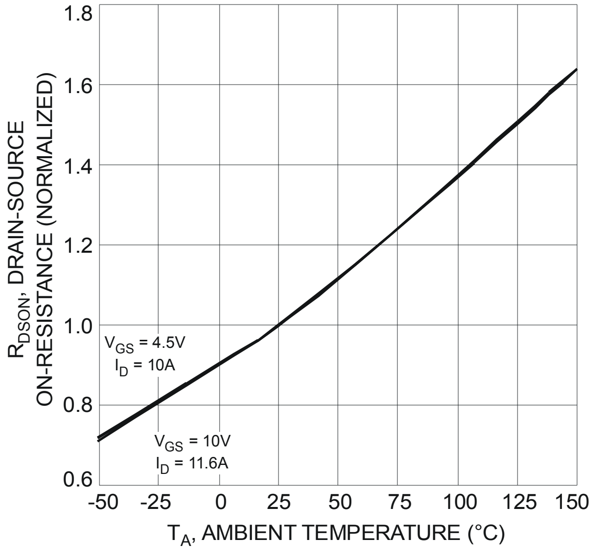


Fig. 5 On-Resistance Variation with Temperature

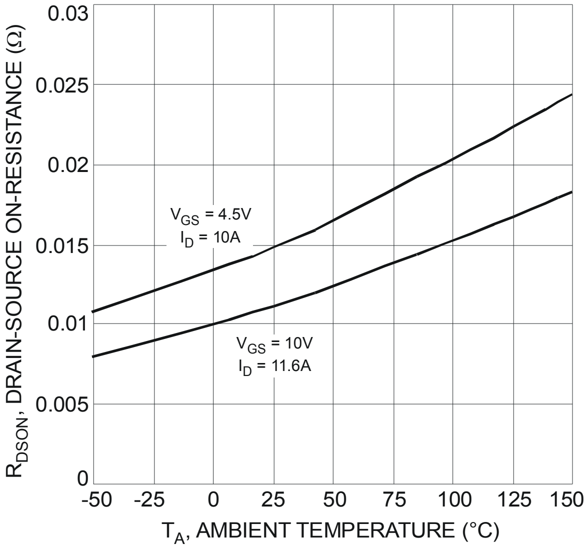


Fig. 6 On-Resistance Variation with Temperature

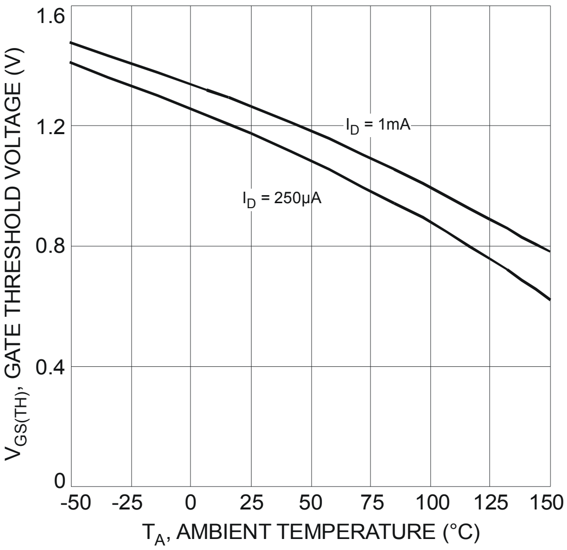


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

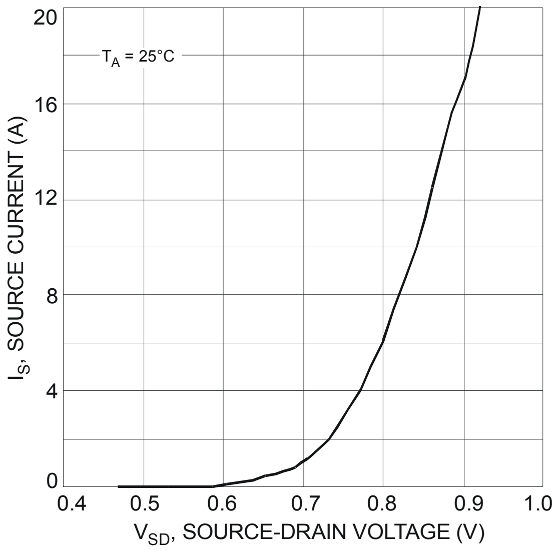


Fig. 8 Diode Forward Voltage vs. Current

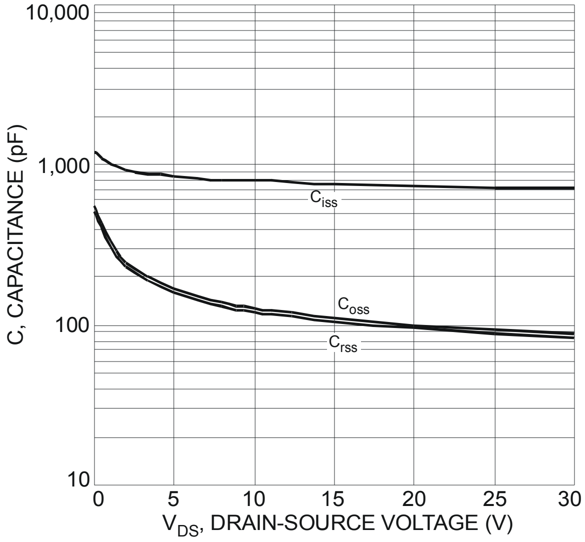


Fig. 9 Typical Total Capacitance

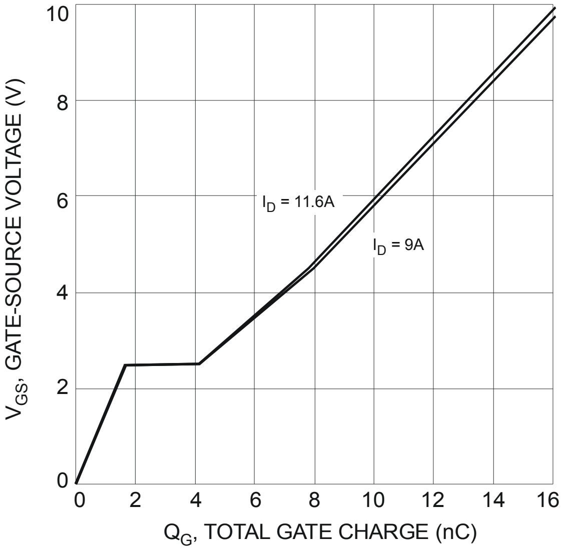


Fig. 10 Total Gate Charge

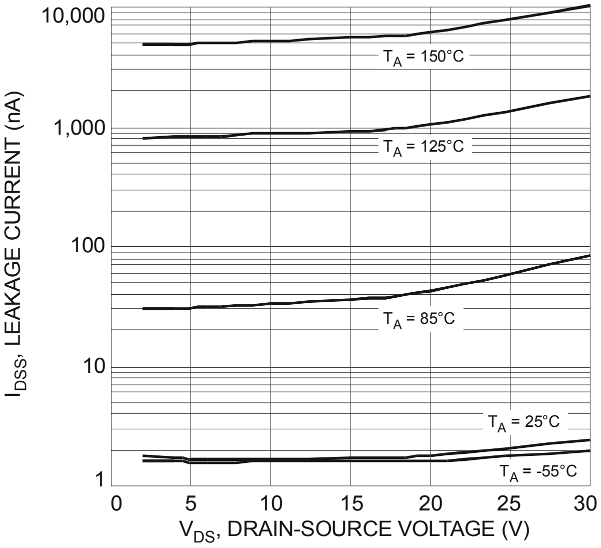


Fig. 11 Typical Leakage Current vs. Drain-Source Voltage

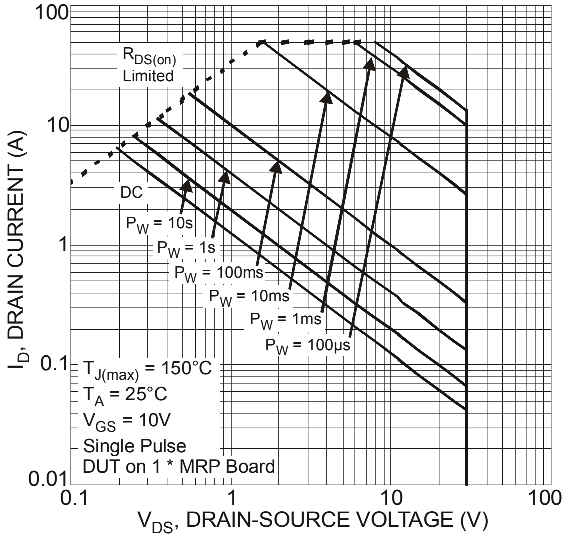


Fig. 12 SOA, Safe Operation Area

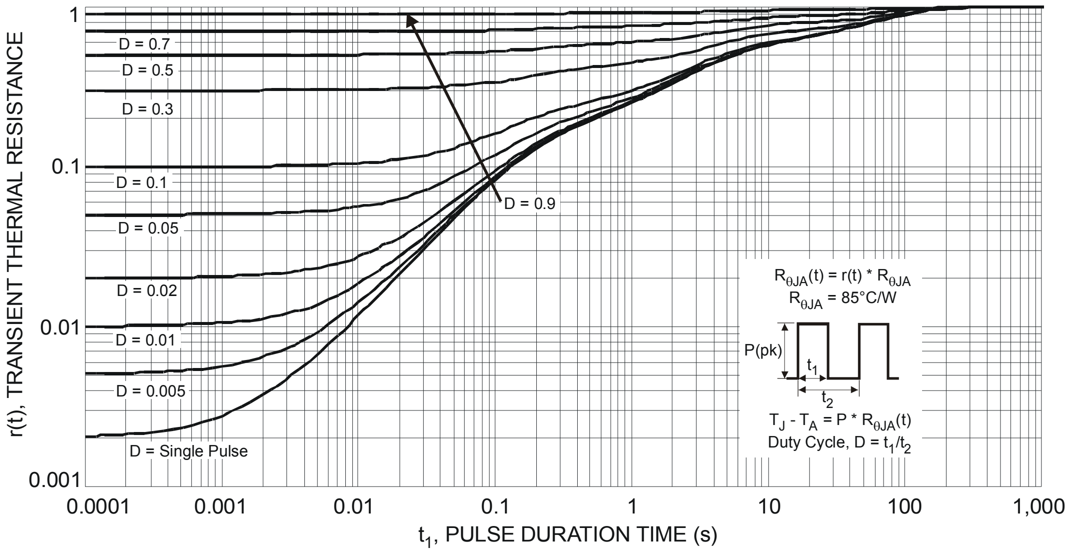
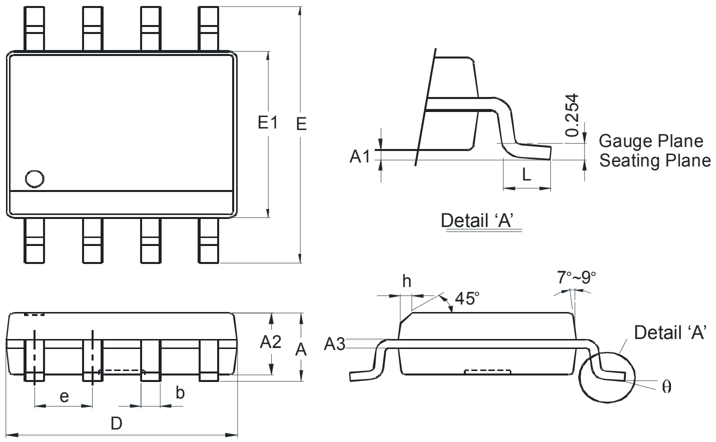


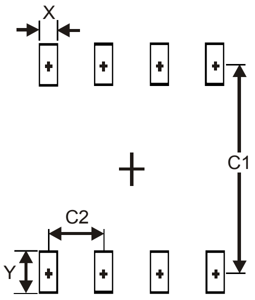
Fig. 13 Transient Thermal Response

Package Outline Dimensions



SO-8		
Dim	**Min**	**Max**
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27