



YOUSHANG SEMICONDUCTOR

**设计研发新型功率器件**

**各类小信号开关**

**中低压及高压大电流等场效应管**

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## Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	$I_D$ $T_A = +25^\circ\text{C}$
50V	$1.8\Omega @ V_{GS} = 10V$	500mA
	$2.0\Omega @ V_{GS} = 4.5V$	450mA

## Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

## Description and Applications

This new generation MOSFET has been designed to minimize the on-state resistance ( $R_{DS(ON)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Backlighting
- DC-DC Converters
- Power Management Functions

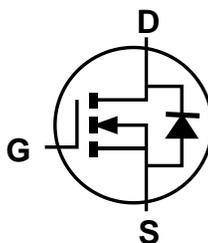
## Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Alloy 42 Leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Weight: 0.008 grams (Approximate)

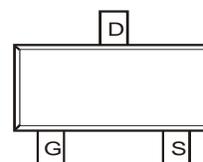


SOT23

Top View



Internal Schematic



Top View

## Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V <sub>DSS</sub>	50	V
Gate-Source Voltage			V <sub>GSS</sub>	±20	V
Continuous Drain Current @ T <sub>SP</sub> = +25°C (Note 5)	Steady State	T <sub>A</sub> = +25°C	I <sub>D</sub>	500	mA
		T <sub>A</sub> = +100°C		300	
Pulsed Drain Current @ T <sub>SP</sub> = +25°C (Notes 5 & 6)			I <sub>DM</sub>	1.2	A

## Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation, @T <sub>A</sub> = +25°C (Note 5)	P <sub>D</sub>	600	mW
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = +25°C (Note 5)	R <sub>θJA</sub>	200	°C/W
Power Dissipation, @T <sub>SP</sub> = +25°C (Note 5)	P <sub>D</sub>	920	mW
Thermal Resistance, @T <sub>SP</sub> = +25°C (Note 5)	R <sub>θJSP</sub>	136	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

## Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	50	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	—	—	0.5	μA	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V
Gate-Body Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	0.4	1.0	1.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	1.3 1.6	1.8 2.0	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.22A V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 0.1A
Forward Transfer Admittance	Y <sub>fs</sub>	40	320	—	mS	V <sub>DS</sub> = 10V, I <sub>D</sub> = 0.1A
Diode Forward Voltage	V <sub>SD</sub>	—	1.0	1.5	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 180mA
Source (Diode Forward) Current	I <sub>S</sub>	—	—	194	mA	T <sub>SP</sub> = +25°C
Peak Source (Diode Forward) Current	I <sub>SM</sub>	—	—	1.2	A	T <sub>SP</sub> = +25°C
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	21.8	40	pF	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	5.6	15	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	3.3	10	pF	
Gate Resistance	R <sub>g</sub>	—	49	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge	Q <sub>g</sub>	—	800	—	pC	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 25V, I <sub>D</sub> = 250mA
Gate-Source Charge	Q <sub>gs</sub>	—	100	—	pC	
Gate-Drain Charge	Q <sub>gd</sub>	—	100	—	pC	
Turn-On Delay Time	t <sub>D(ON)</sub>	—	2.93	—	ns	V <sub>DD</sub> = 30V, V <sub>GEN</sub> = 10V, R <sub>L</sub> = 150Ω, R <sub>GEN</sub> = 50Ω, I <sub>D</sub> = 0.2A
Turn-On Rise Time	t <sub>R</sub>	—	2.99	—	ns	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	9.45	—	ns	
Turn-Off Fall Time	t <sub>F</sub>	—	8.3	—	ns	

- Notes:
- Device mounted on FR-4 PCB, with minimum recommended pad layout.
  - Repetitive rating, pulse width limited by junction temperature.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.

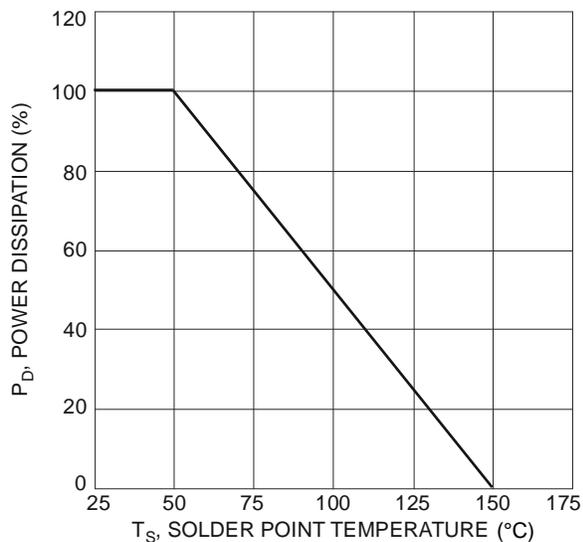


Fig 1. Normalized Total Power Dissipation as a Function of Solder Point Temperature

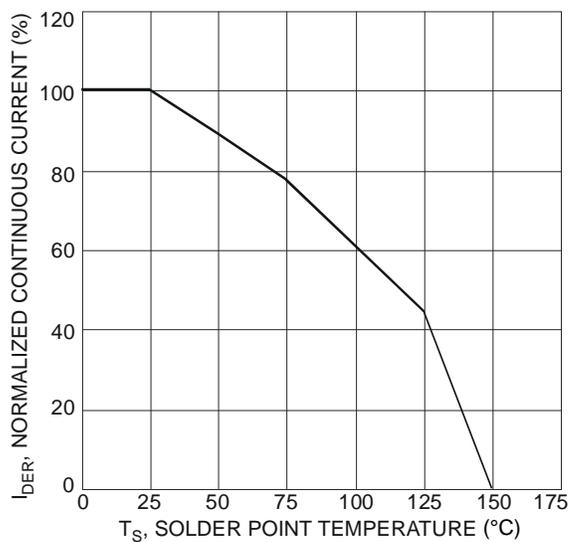


Fig 2. Normalized Continuous Current vs. Solder Point Temperature

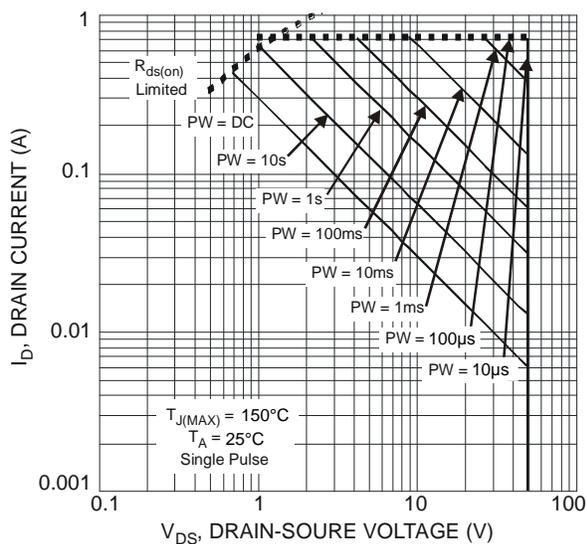


Fig 3 SOA, Safe Operation Area

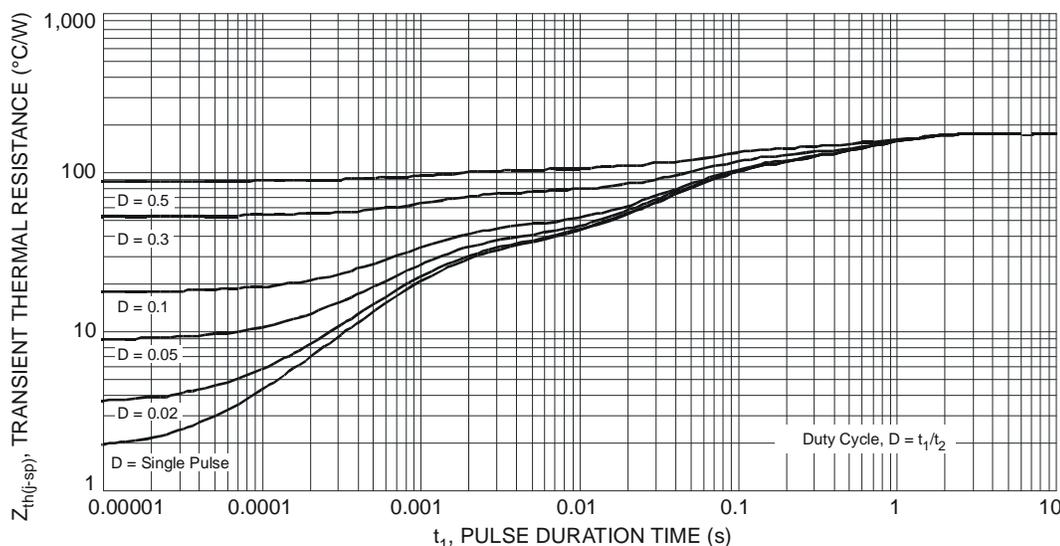


Fig. 4 Transient Thermal Response

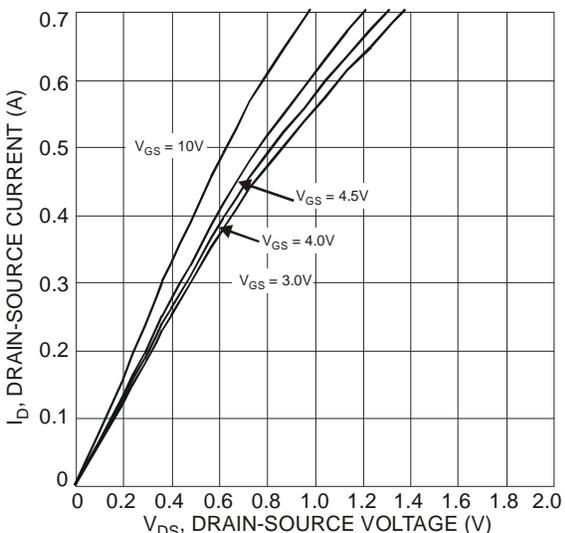


Fig. 5 Drain-Source Current vs. Drain-Source Voltage

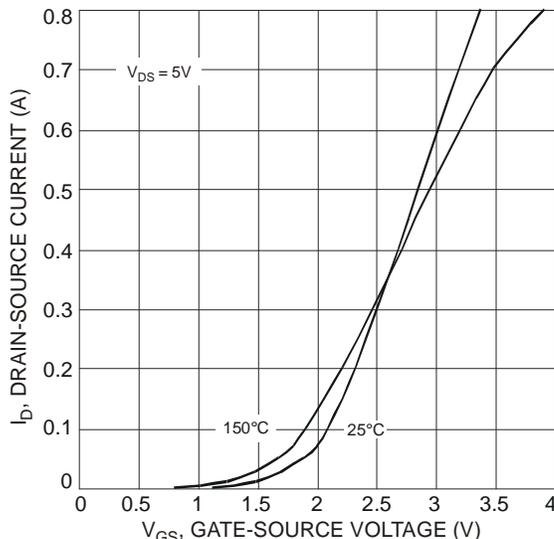


Fig. 6 Transfer Characteristics

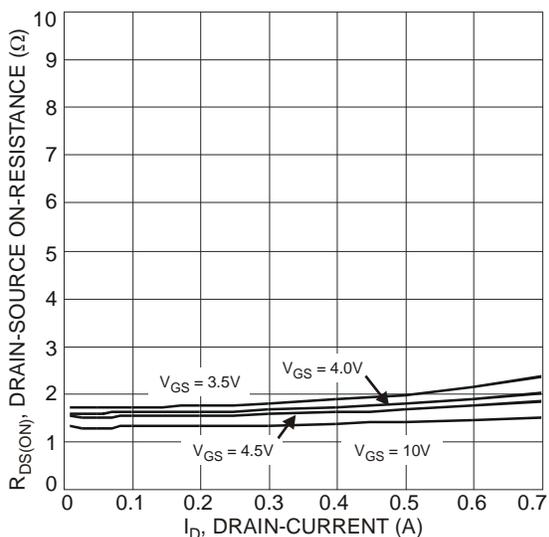


Fig. 7 Drain-Source On-Resistance vs. Drain-Current

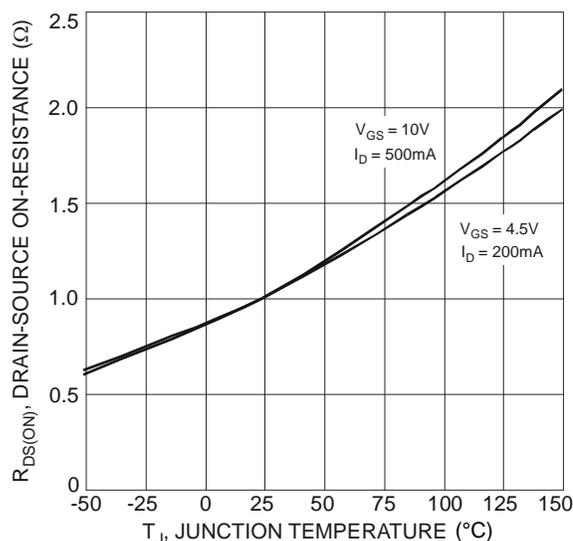


Fig. 8 Drain-Source On-Resistance vs. Junction Temperature

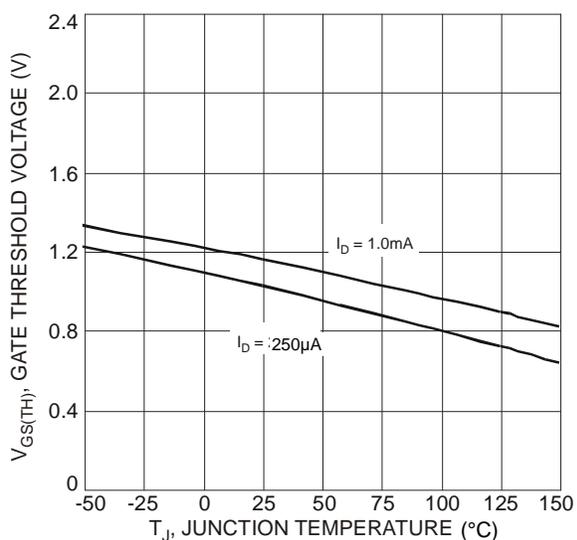


Fig. 9 Gate Threshold Voltage vs. Junction Temperature

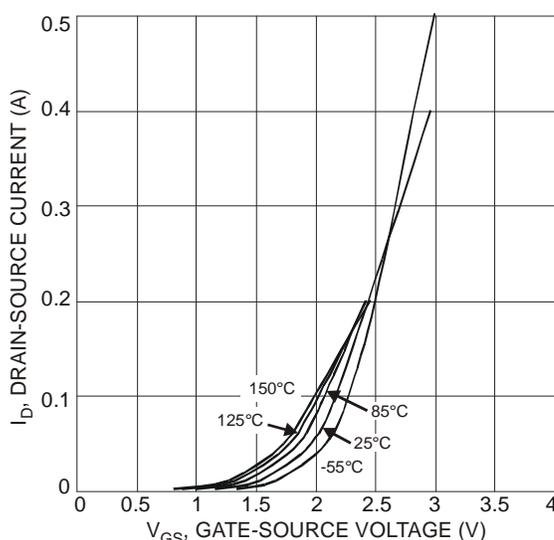


Fig. 10 Transfer Characteristics

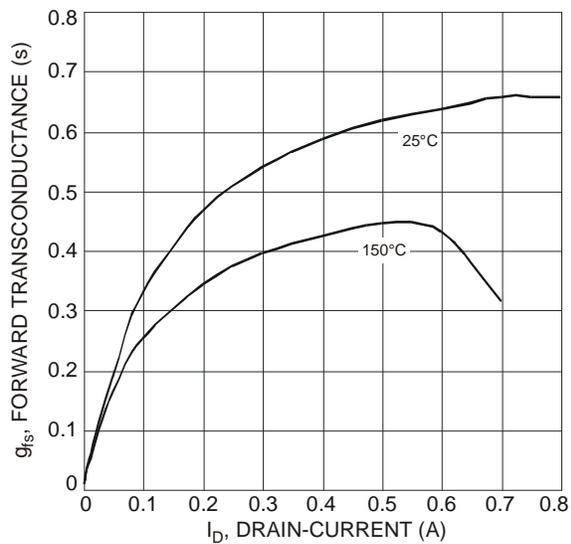


Fig. 11 Typical Transfer Characteristic

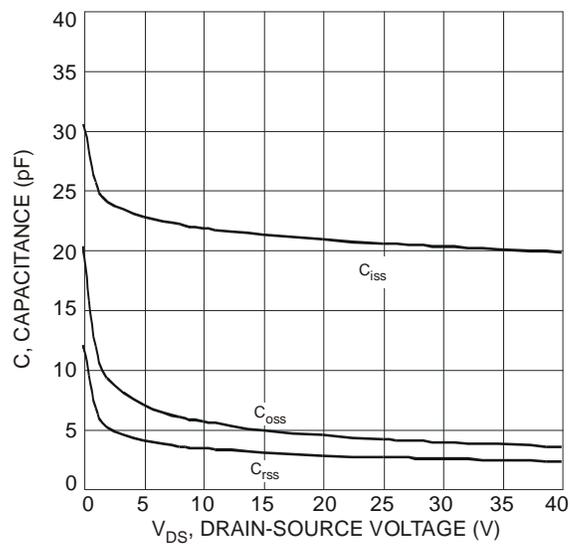


Fig. 12 Capacitance vs. Drain-Source Voltage

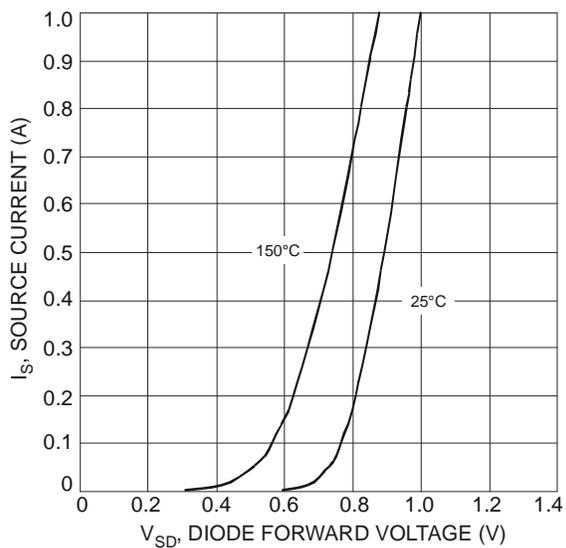
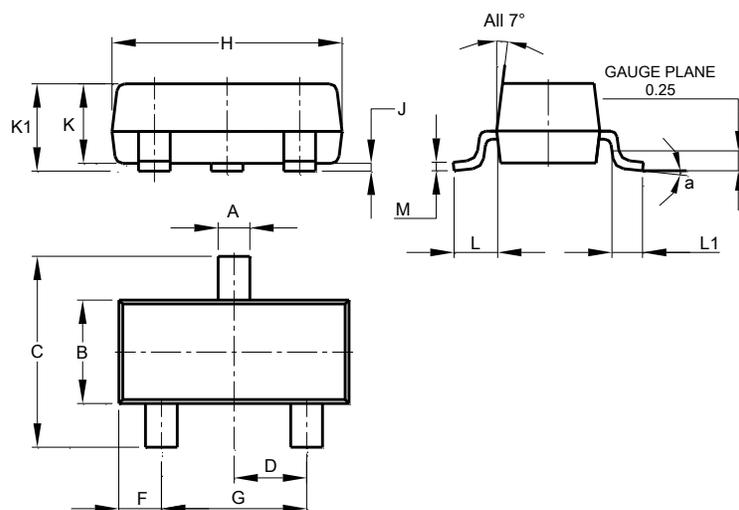


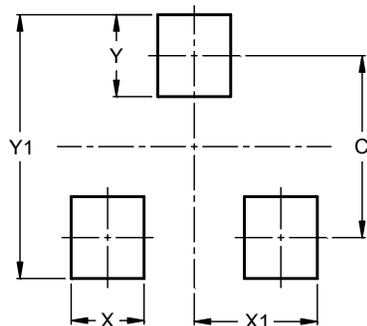
Fig. 13 Source Current vs. Diode Forward Voltage

## Package Outline Dimensions

**SOT23**


SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	0°	8°	--
All Dimensions in mm			

## Suggested Pad Layout

**SOT23**


Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9