



YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Product Summary

$V_{(BR)DSS}$	$R_{DS(ON) \max}$	$I_D \max$ $T_A = +25^\circ C$
30V	23m Ω @ $V_{GS} = 10V$	10A
	33m Ω @ $V_{GS} = 4.5V$	8A

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

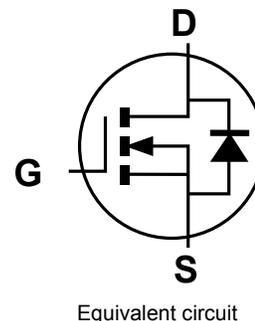
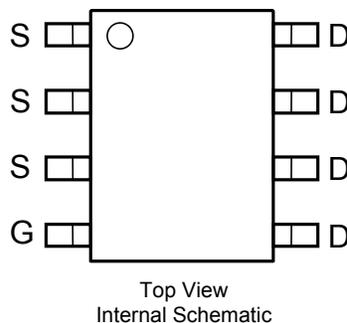
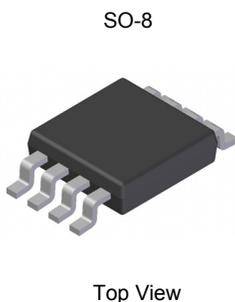
- Backlighting
- Power Management Functions
- DC-DC Converters

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Low Gate Resistance

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.074 grams (approximate)



Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	± 25	V
Continuous Drain Current (Note 5)	Steady State	$T_A = +25^\circ\text{C}$	I_D	10	A
		$T_A = +85^\circ\text{C}$		6	
Pulsed Drain Current (Note 5)			I_{DM}	60	A
Avalanche Current (Notes 6)			I_{AR}	16	A
Repetitive Avalanche Energy (Notes 6) $L = 0.1\text{mH}$			E_{AR}	12.8	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	1.42	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$ (Note 5)	$R_{\theta JA}$	88.4	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.45	2.4	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	15	23	m Ω	$V_{GS} = 10\text{V}, I_D = 10\text{A}$
			25	33		$V_{GS} = 4.5\text{V}, I_D = 7.5\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	—	2.5	—	S	$V_{DS} = 5\text{V}, I_D = 10\text{A}$
Diode Forward Voltage	V_{SD}	—	0.69	1	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	478.9	—	pF	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	96.7	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	61.4	—	pF	
Gate Resistance	R_g	0.4	1.1	1.6	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	5.0	8	nC	$V_{DS} = 15\text{V}, V_{GS} = 10\text{V}, I_D = 10\text{A}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	10.5	17		
Gate-Source Charge	Q_{gs}	—	1.8	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.6	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	2.9	—	ns	
Turn-On Rise Time	t_r	—	7.9	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	14.6	—	ns	$V_{GS} = 10\text{V}, V_{DS} = 15\text{V}, R_G = 3\Omega, R_L = 1.5\Omega$
Turn-Off Fall Time	t_f	—	3.1	—	ns	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - I_{AR} and E_{AR} rating are based on low frequency and duty cycles to keep $T_J = +25^\circ\text{C}$
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

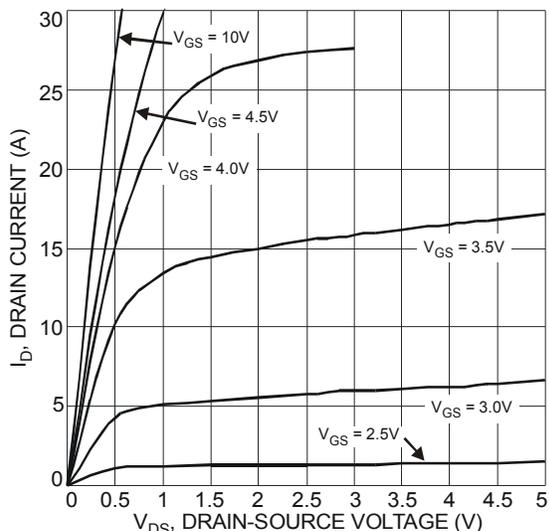


Fig. 1 Typical Output Characteristic

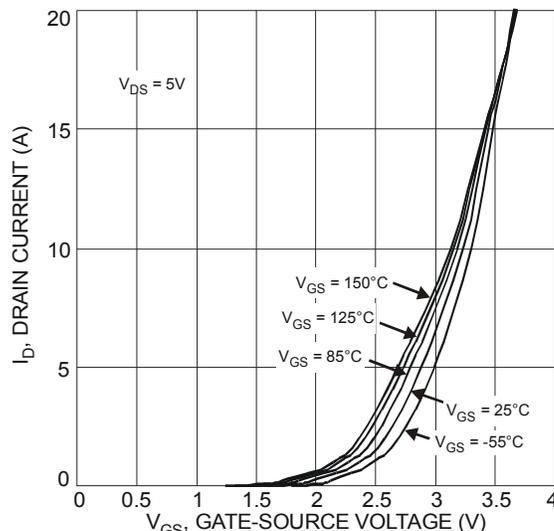


Fig. 2 Typical Transfer Characteristic

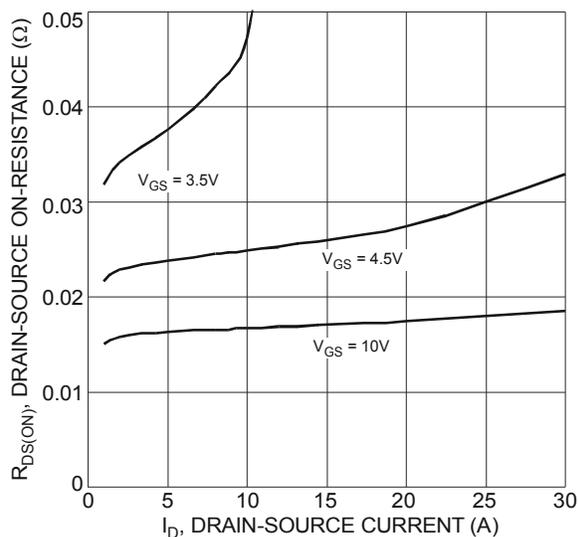


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

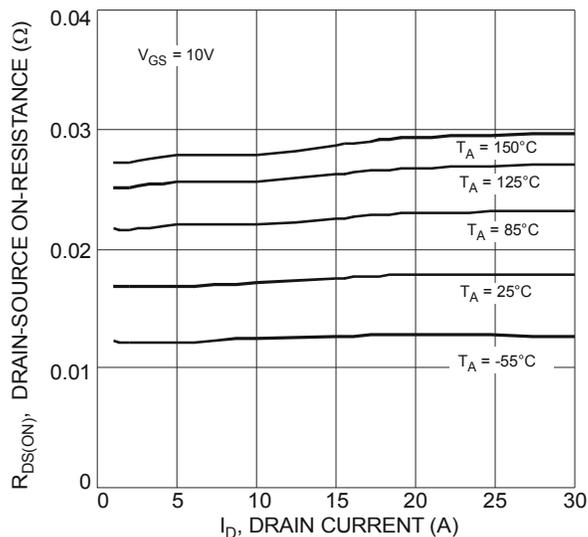


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

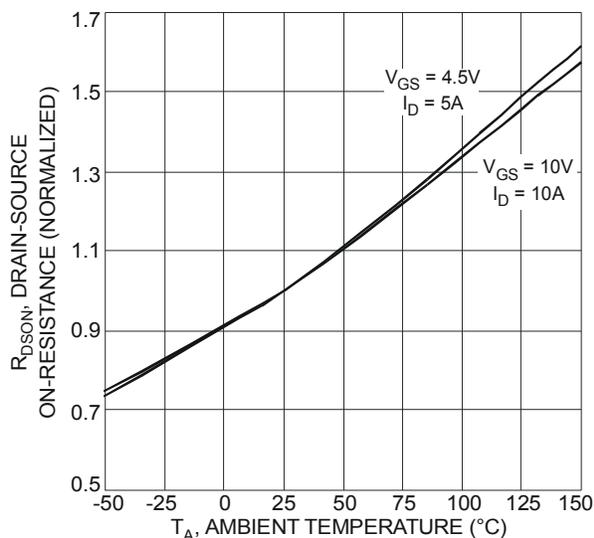


Fig. 5 On-Resistance Variation with Temperature

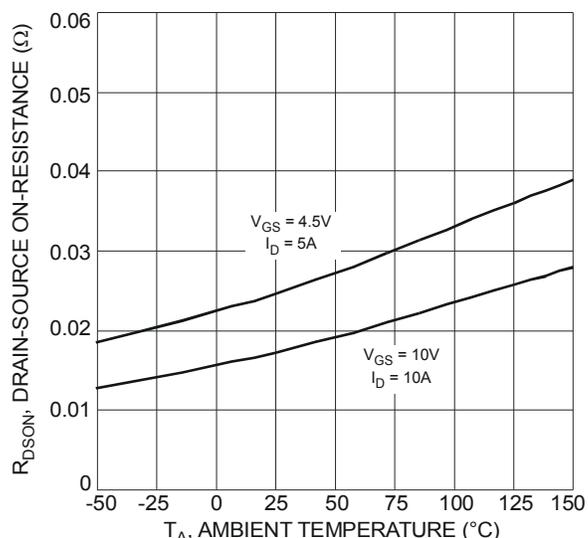


Fig. 6 On-Resistance Variation with Temperature

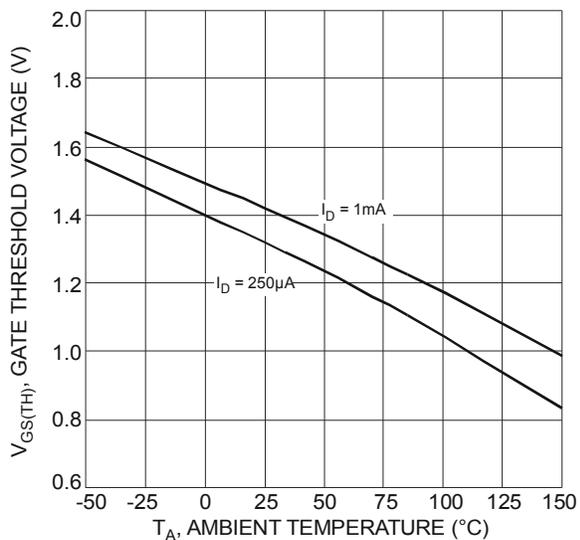


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

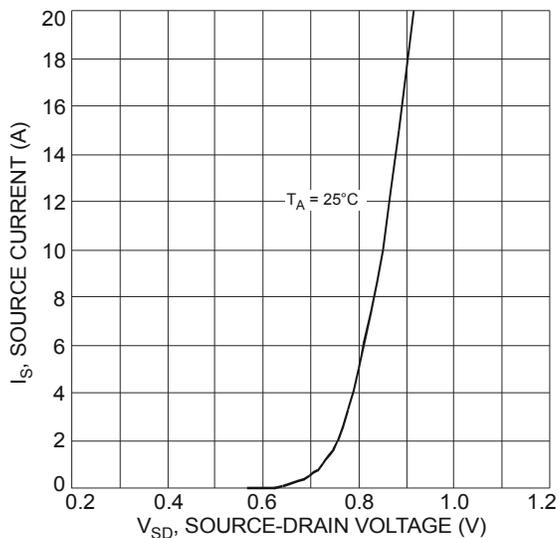


Fig. 8 Diode Forward Voltage vs. Current

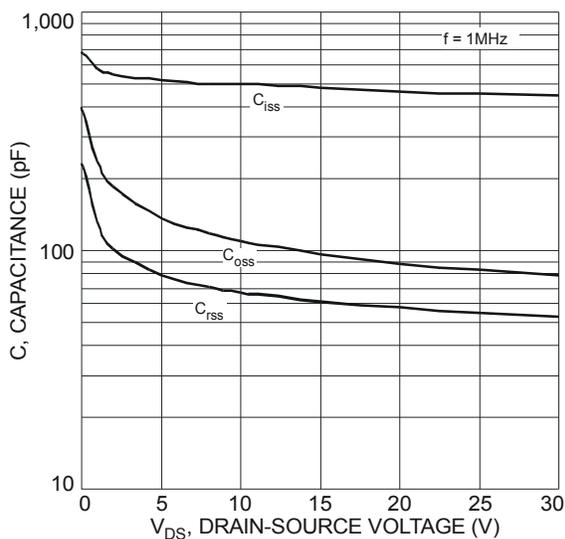


Fig. 9 Typical Total Capacitance

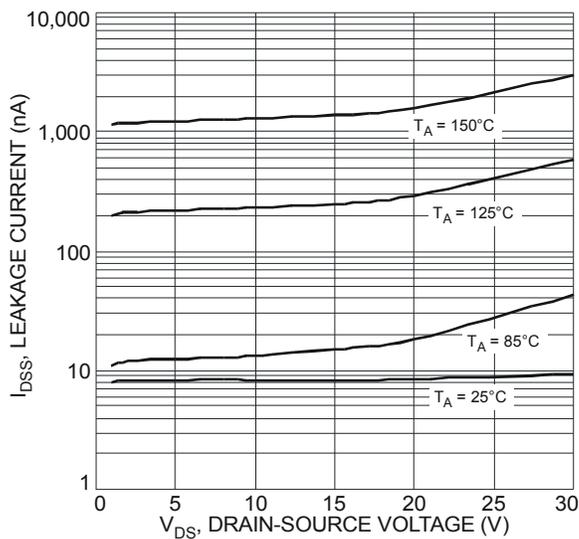


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

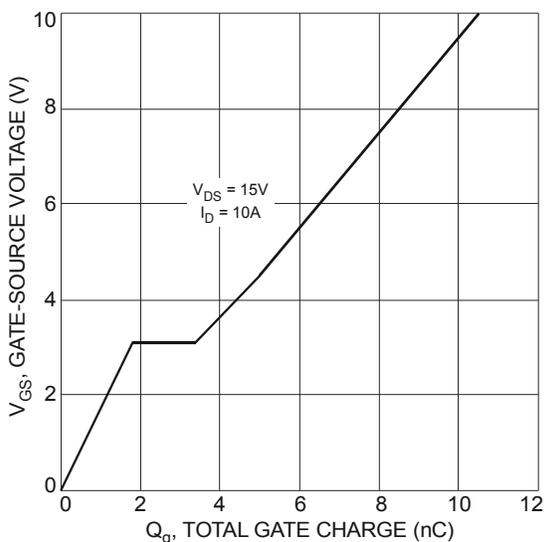


Fig. 11 Gate-Charge Characteristics

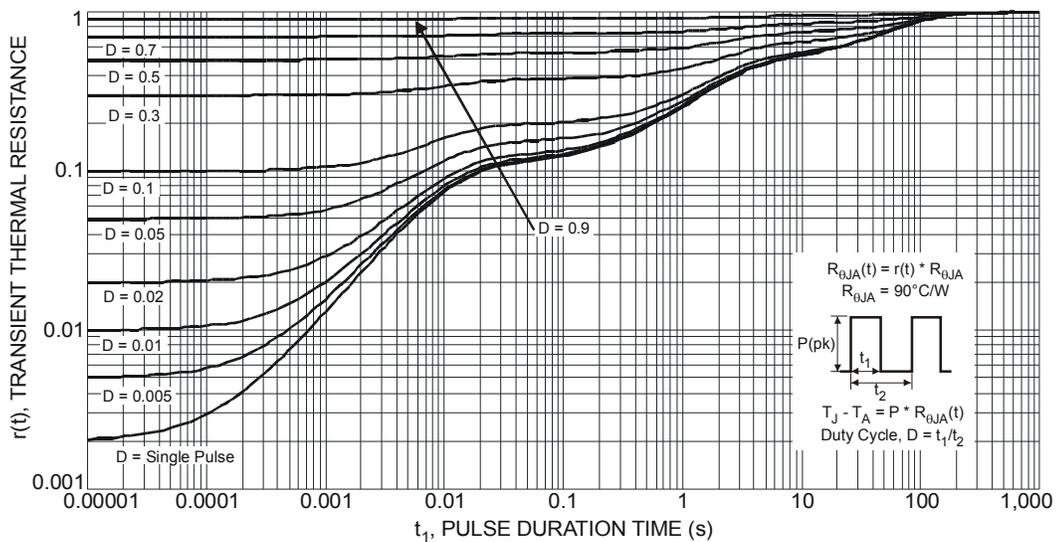
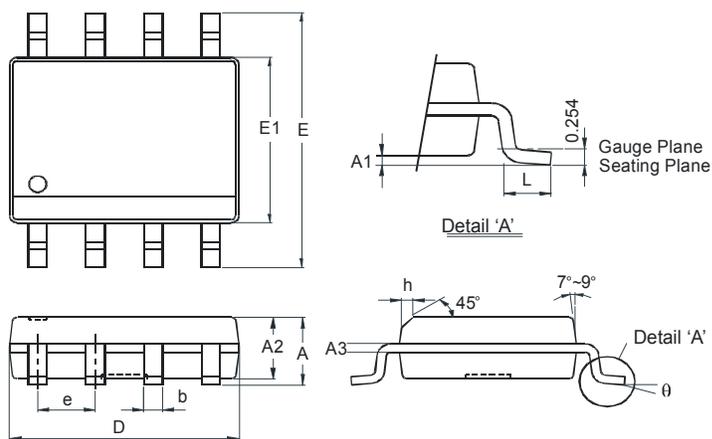


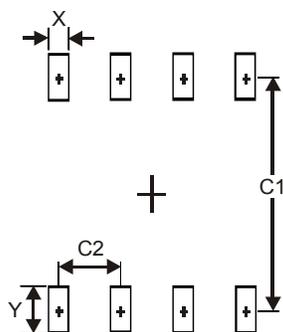
Fig. 12 Transient Thermal Response

Package Outline Dimensions



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27