优尚

YOUSHANG SEMICONDUCTOR

设计研发新型功率器件

各类小信号开关

中低压及高压大电流等场效应管

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Description

NK-ZXGD3108N8 is a 40V Active OR'ing MOSFET Controller designed for driving a very low $R_{DS(ON)}$ Power MOSFET as an ideal diode. This replaces the standard rectifier to reduce the forward voltage drop and overall increase the power transfer efficiency.

The NK-ZXGD3108N8 can be used on both high-side and low-side power supply units (PSU) with rails up to ±40V. It enables very low $R_{DS(ON)}$MOSFETs to operate as ideal diodes as the turn-off threshold is only -3mV with ±2mV tolerance. In the typical 12V configuration, the standby power consumption is <5mW as the low quiescent supply current is <400µA. During PSU fault condition, the OR'ing Controller detects the power reduction and rapidly turns off the MOSFET in <600ns to block reverse current flow and avoid the common bus voltage dropping.

Features

- Active OR'ing MOSFET Controller for High- or Low-Side PSU
- Ideal Diode to Reduce Forward Voltage Drop
- -3mV Typical Turn-Off Threshold with ±2mV Tolerance
- 40V Drain Voltage Rating
- 25V V_{CC} Rating
- <5mW Standby Power with Quiescent Supply Current <400µA
- <600ns Turn-Off Time to Minimize Reverse Current

Applications

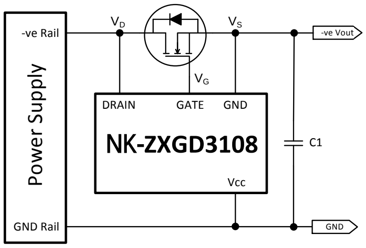
Active OR'ing Controller in:

- (N+1) Redundant Power Supplies
- Telecom and Networking
- Data Centers and Servers

Mechanical Data

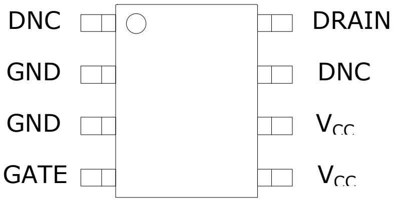
- Case: SO-8
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (Approximate)

Typical Configuration for Low-Side -ve Supply Rail



SO-8

Top View



Pin Name	Pin Function
DNC	Do Not Connect
GND	Power Ground
GATE	Gate Drive
DRAIN	Drain Sense
V_{CC}	Power Supply

Absolute Maximum Ratings (Voltage relative to GND, @ T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	25	V
Drain Pin Voltage	V_D	-3 to 40	V
Gate Output Voltage	V_G	-3 to V_{CC} +3	V
Gate Driver Peak Source Current	I_{SOURCE}	2	A
Gate Driver Peak Sink Current	I_{SINK}	5	A

Thermal Characteristics (@ T_A = +25°C, unless otherwise specified.)

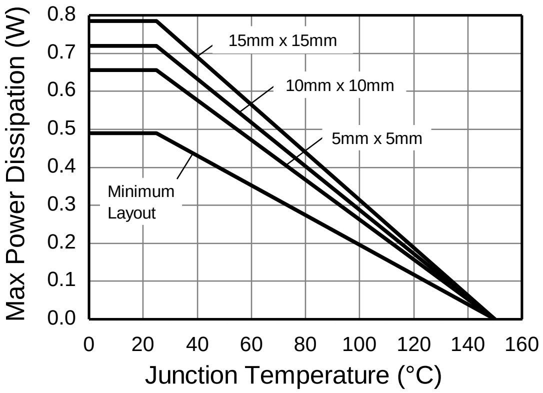
Characteristic		Symbol	Value	Unit
Power Dissipation Linear Derating Factor	(Note 5)	P_D	490 3.92	mW mW/°C
	(Note 6)		655 5.24	
	(Note 7)		720 5.76	
	(Note 8)		785 6.28	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	255	°C/W
	(Note 6)		191	
	(Note 7)		173	
	(Note 8)		159	
Thermal Resistance, Junction to Lead	(Note 9)	$R_{\theta JL}$	135	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-50 to +150	°C

ESD Ratings (Note 10)

Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge – Human Body Model	ESD HBM	2,000	V	2
Electrostatic Discharge – Machine Model	ESD MM	200	V	B

Notes:
5. For a device surface mounted on minimum recommended pad layout FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
6. Same as Note (5), except pins 2 & 3 (GND) and pins 5 & 6 (V_{CC}) are both connected to separate 5mm x 5mm 1oz copper heat-sinks.
7. Same as Note (6), except both heat-sinks are 10mm x 10mm.
8. Same as Note (6), except both heat-sinks are 15mm x 15mm.
9. Thermal resistance from junction to solder-point at the end of each lead on pins 2 & 3 (GND) and pins 5 & 6 (V_{CC}).
10. Refer to JEDEC specification JESD22-A114 and JESD22-A11

Thermal Derating Curve



Derating Curve

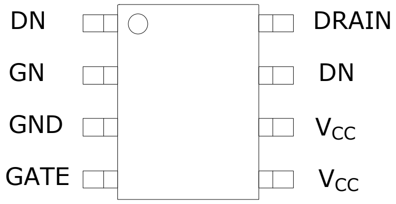
Electrical Characteristics (@ V_{CC} = 12V, T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition	
Input Supply							
Operating Supply Voltage	V_{CC}	4	—	20	V		
Quiescent Current	I_Q	—	200	400	µA	-0.6V ≤ V_{DRAIN} ≤ 30V	
Gate Driver							
Gate Peak Source Current	I_{SOURCE}	—	0.66	—	A	C_L = 47nF	
Gate Peak Sink Current	I_{SINK}	—	3.3	—			
Gate Peak Source Current (Note 11)	I_{SOURCE}	1	—	—	A	V_{GATE} = 5V & V_{DRAIN} = -1V	
Gate Peak Sink Current (Note 11)	I_{SINK}	1.8	—	—	A	V_{GATE} = 5V & V_{DRAIN} = 1V	
Detector Under DC Condition							
Turn-Off Threshold Voltage	V_T	-5	-3	-1	mV	V_G ≤1V	Load: 50nF Capacitor Connected in Parallel with 50kΩ Resistor
Gate Output Voltage	$V_{G(OFF)}$	—	0.1	0.3	V	V_{DRAIN} ≥ 0mV	
	V_G	10.5	10.9			V_{DRAIN} = -8mV	
	$V_{G(OFF)}$	—	0.1	0.3		V_{DRAIN} ≥ 0mV & V_{CC} = 4V	
	V_G	2.5	2.9	—		V_{DRAIN} = -8mV & V_{CC} = 4V	
	$V_{G(OFF)}$	—	0.1	0.3		V_{DRAIN} ≥ -8mV & V_{CC} = 20V	
	V_G	18.5	18.8	—		V_{DRAIN} = -8mV & V_{CC} = 20V	
Switching Performance							
Turn-On Propagation Delay	$t_{D(RISE)}$	—	400	—	ns	C_L = 47nF Rise and Fall Measured 10% to 90% Refer to Application Test Circuit Below	
Gate Rise Time	t_R	—	695	—			
Turn-Off Propagation Delay	$t_{D(FALL)}$	—	400	—			
Gate Fall Time	t_F	—	131	—			

Note: 11. Measured under pulsed conditions. Pulse width = 300µs. Duty cycle ≤ 2%.

Pin Functions

Pin Number	Pin Name	Pin Function and Description
1, 7	DNC	**Do Not Connect** Leave pin floating.
2, 3	GND	**Ground** Connect this pin to the MOSFET source terminal and ground reference point.
4	GATE	**Gate Drive** This pin sources (I_{SOURCE}) and sinks (I_{SINK}) current into the MOSFET gate. The turn-on time of the MOSFET can be programmed through an external gate resistor (R_G).
5, 6	V_{CC}	**Power Supply** This supply pin should be closely decoupled to ground with a X7R type capacitor.
8	DRAIN	**Drain Sense** Connect this pin to the MOSFET drain terminal to detect the change in drain-source voltage.

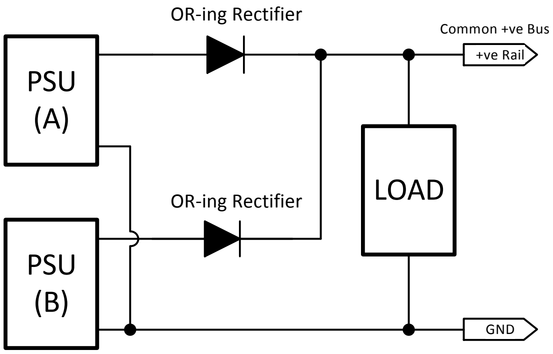


Layout Considerations

The GATE Pin should be close to the MOSFET gate to minimize trace resistance and inductance to maximize switching performance. While the V_{CC} to GND Pin needs an X7R type capacitor closely decoupling the supply. Trace widths should be maximized in the high current paths through the MOSFET and ground return loop in order to minimize the effects of circuit resistance and inductance. The ground return loop should also be as short as possible.

For thermal consideration, the main heat path is from pins 2 and 3 (GND), and pins 5 and 6 (V_{CC}). For best thermal performance, connect the copper area to pins 2 and 3 (GND), and pins 5 and 6 (V_{CC}) should be maximized.

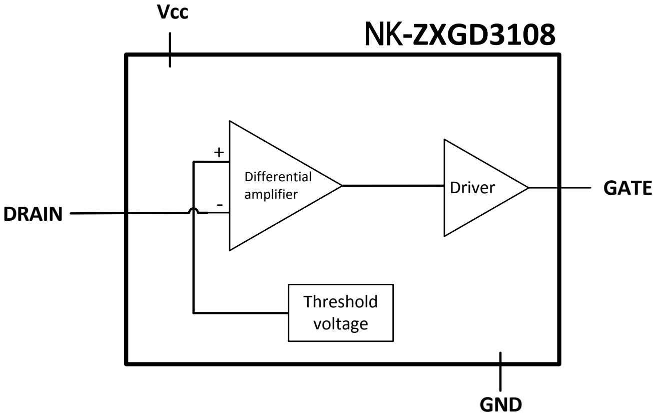
Active OR'ing or (N+1) Redundancy Application



Critical systems require fault-tolerant power supply that can be achieved by paralleling two or more PSUs into (N+1) redundancy configuration. During normal operation, usually all PSUs equally share the load for maximum reliability. If one of the PSU is unplugged or fails, then the other PSUs fully support the load. To avoid the faulty PSU from affecting the common bus, then an OR'ing rectifier blocks the reverse current flow into the faulty PSU. Likewise during hot-swapping, the OR'ing rectifiers isolate a PSU's discharged output capacitors from the common bus.

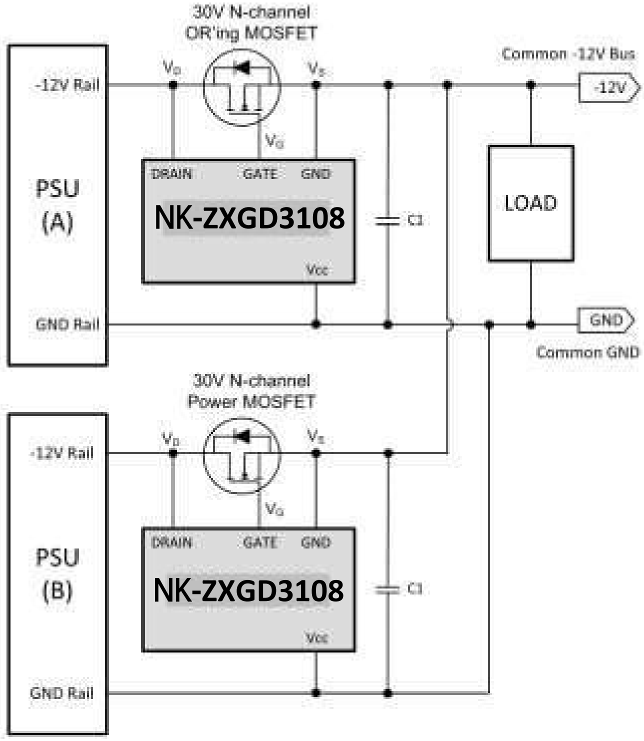
As the load current is in the tens of amps then a standard rectifier has a significant forward voltage drop. This both wastes power and significantly drops the potential on low voltage rails. Hence, very low $R_{DS(ON)}$ Power MOSFETs can replace the standard rectifiers and the NK-ZXGD3108 controls
the MOSFET as an ideal diode.

Functional Block Diagram

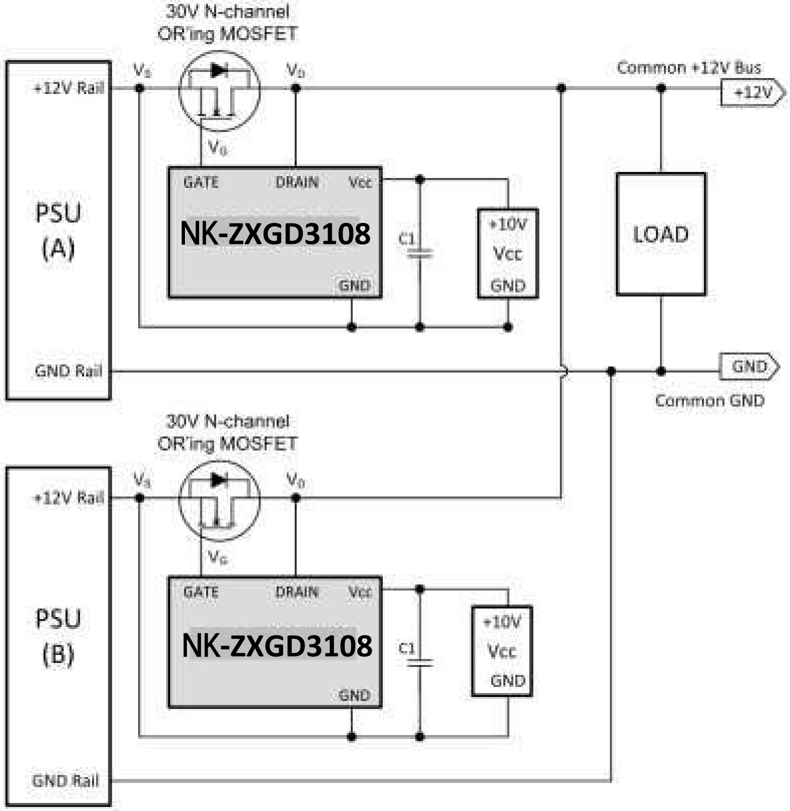


The device is comprised of a differential amplifier and high current driver. The differential amplifier acts as a detector and monitors the DRAIN-to-GND Pin voltage difference. When this difference is less than the threshold voltage (V_T), then a positive output voltage approaching V_{CC} is given on the GATE Pin. Conversely, when the DRAIN-to-GND Pin voltage difference is greater than V_T, then the GATE Pin voltage is rapidly reduced towards the GND voltage.

Typical Application Circuits



Focus Application of the NK-ZXGD3108 OR'ing Controller is for Redundant Low-Side -12V Power Supply Rail

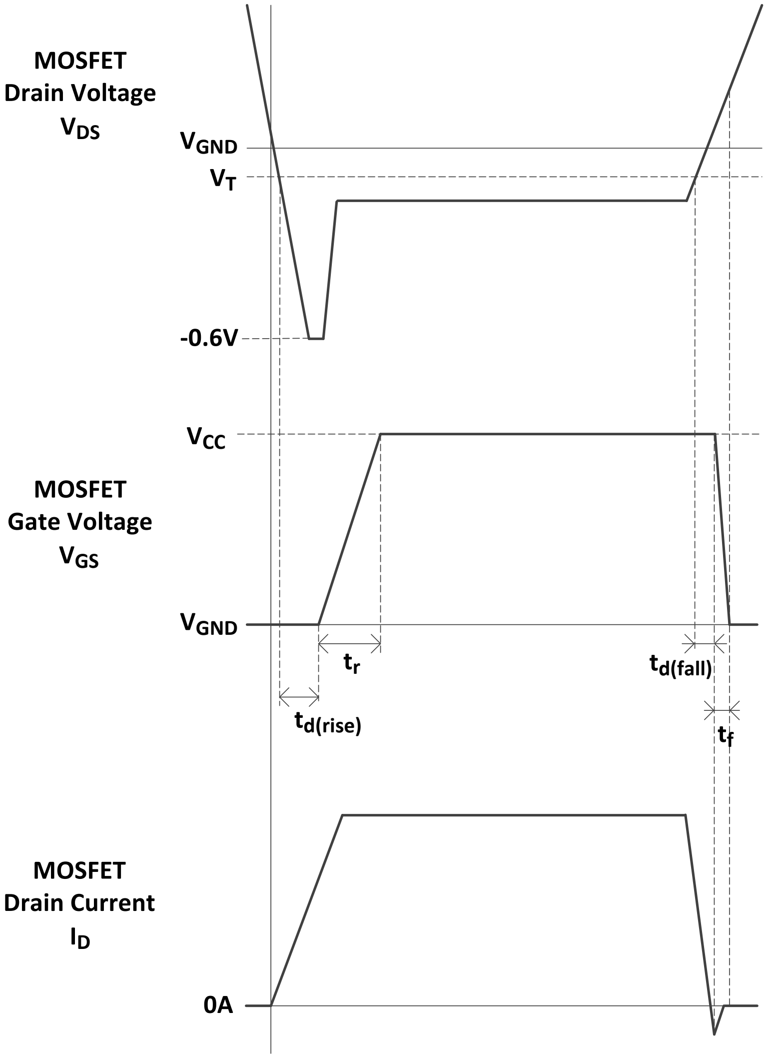


Example of the NK-ZXGD3108 OR'ing Controller in a Redundant High-Side +12V Power Supply Rail with V_{CC} Supply

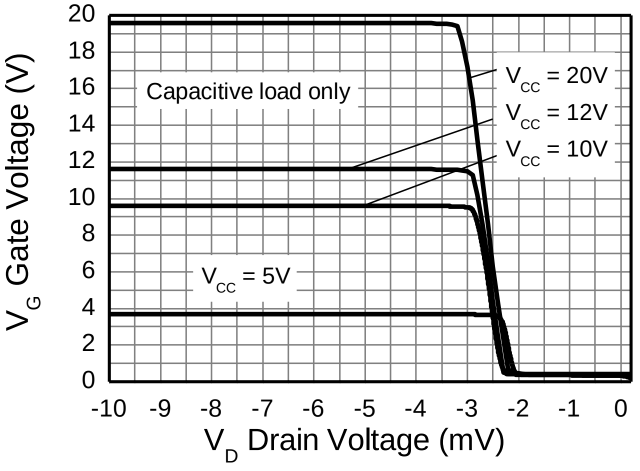
Operation in Typical Application

The NK-ZXGD3108 operation is described step-by-step with reference to the typical application circuits and the timing diagram below:

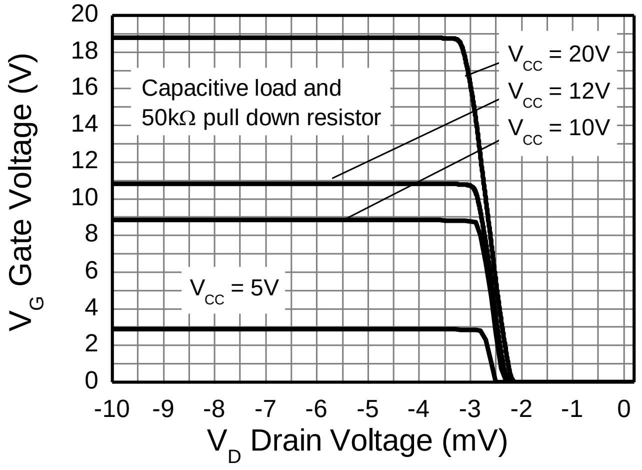
1. The NK-ZXGD3108 differential amplifier monitors the MOSFET's drain-source voltage (V_{DS}).
2. At system start up, the MOSFET body diode is forced to conduct current from the input PSU to the load and V_{DS} is approximately -0.6V as measured by the differential amplifier between DRAIN-to-GND pins.
3. As $V_{DS} < V_T$ (threshold voltage), then the differential amplifier outputs a positive voltage approaching V_{CC} with respect to GND. This feeds the driver stage from which the GATE Pin voltage rises towards V_{CC}.
4. The sourcing current out of the GATE Pin drives the MOSFET gate to enhance the channel and turn it on.
5. If a short condition occurs on the input PSU, it causes the MOSFET V_{DS} to increase.
6. When $V_{DS} > V_T$, then the differential amplifier's output goes to GND and the driver stage rapidly pulls the GATE Pin voltage to GND, turning off the MOSFET channel. This prevents high reverse current flow from the load to the PSU which could pull down the common bus voltage causing catastrophic system failure.



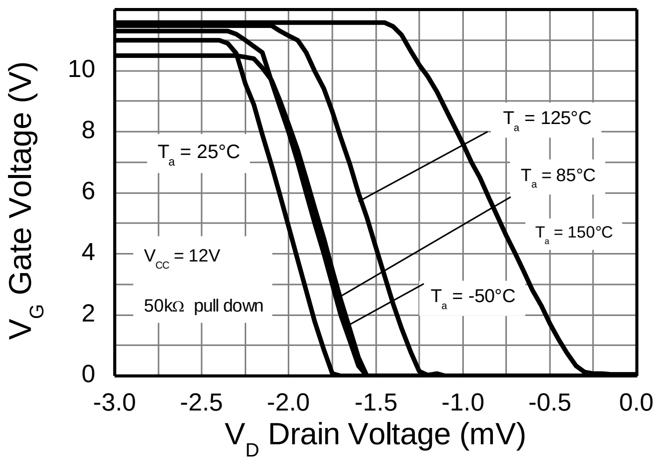
Typical Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)



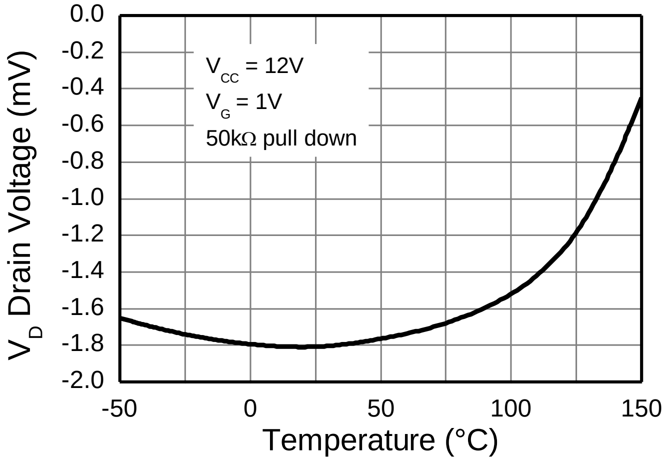
Transfer Characteristic



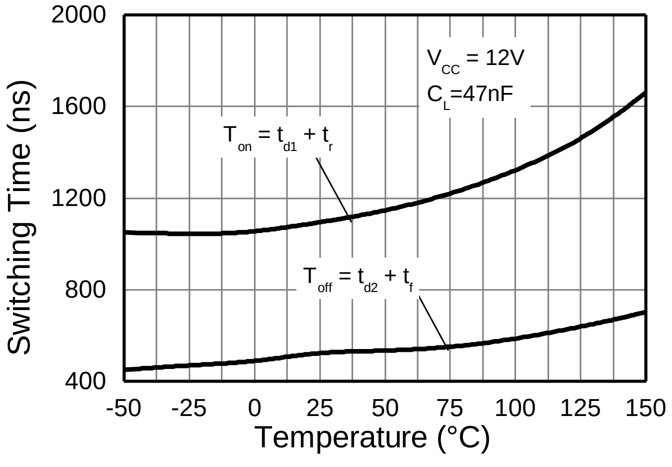
Transfer Characteristic



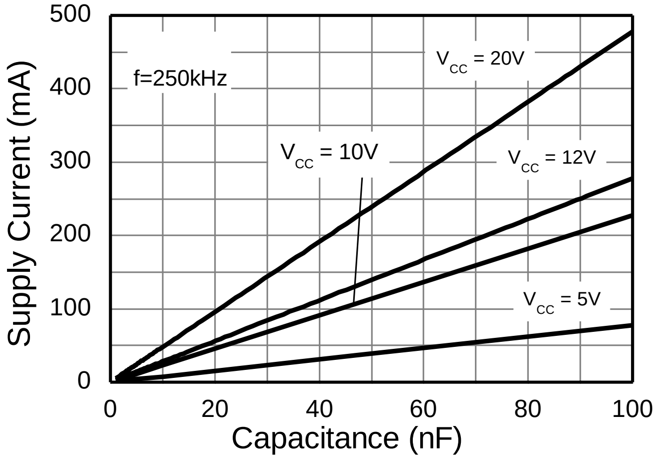
Transfer Characteristic



Drain Sense Voltage vs Temperature

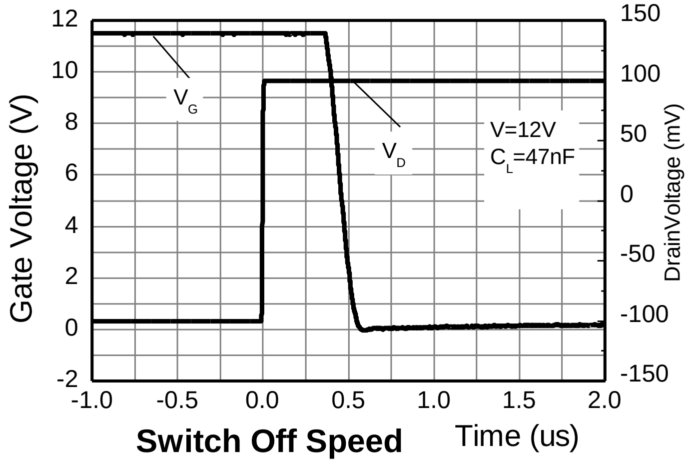


Switching vs Temperature

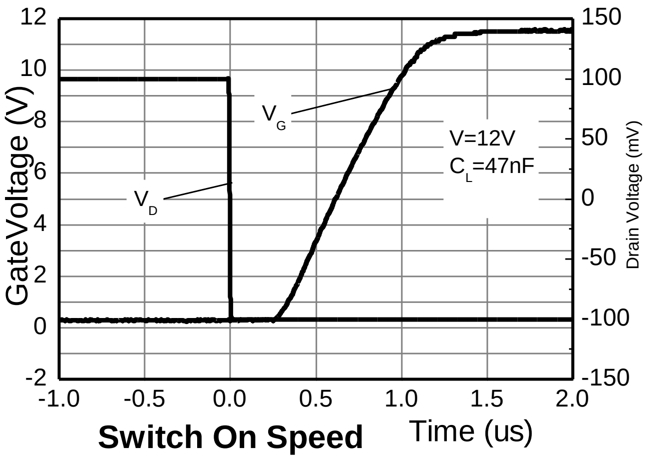


Supply Current vs Capacitive Load

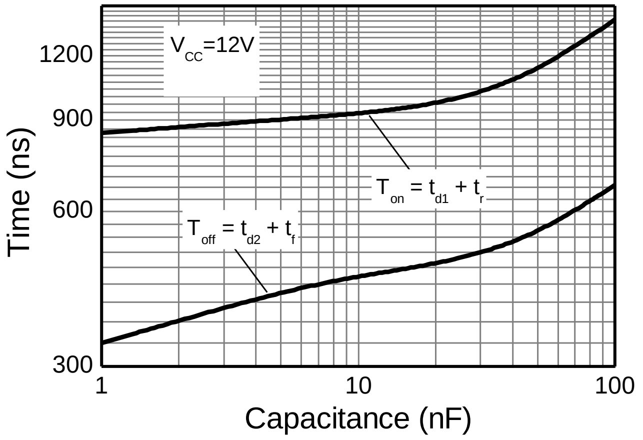
Typical Electrical Characteristics (Continued) (@T_A = +25°C, unless otherwise specified.)



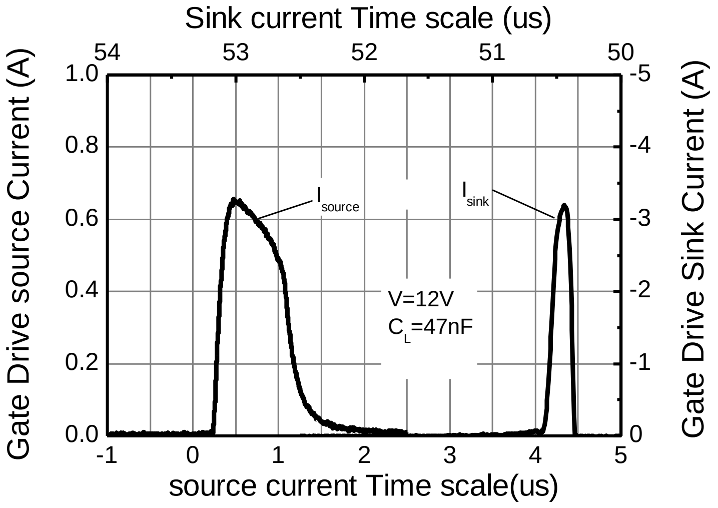
Switch Off Speed



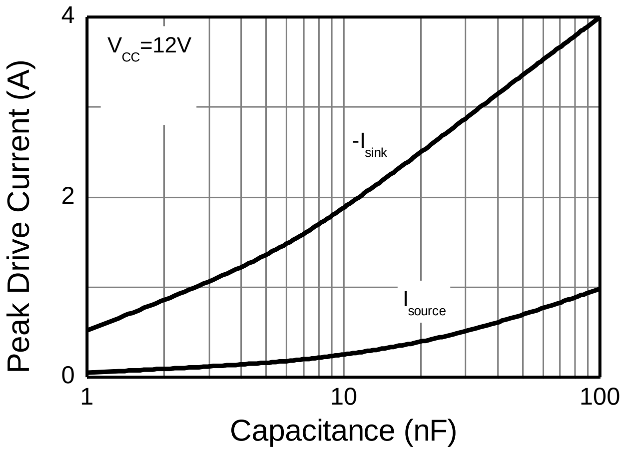
Switch On Speed



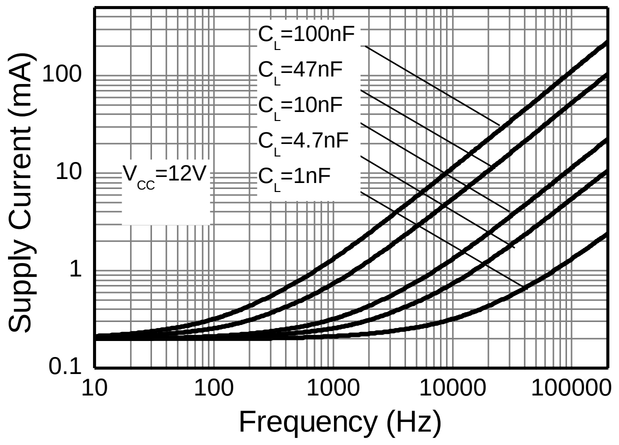
Switching vs Capacitive Load



Gate Drive Current



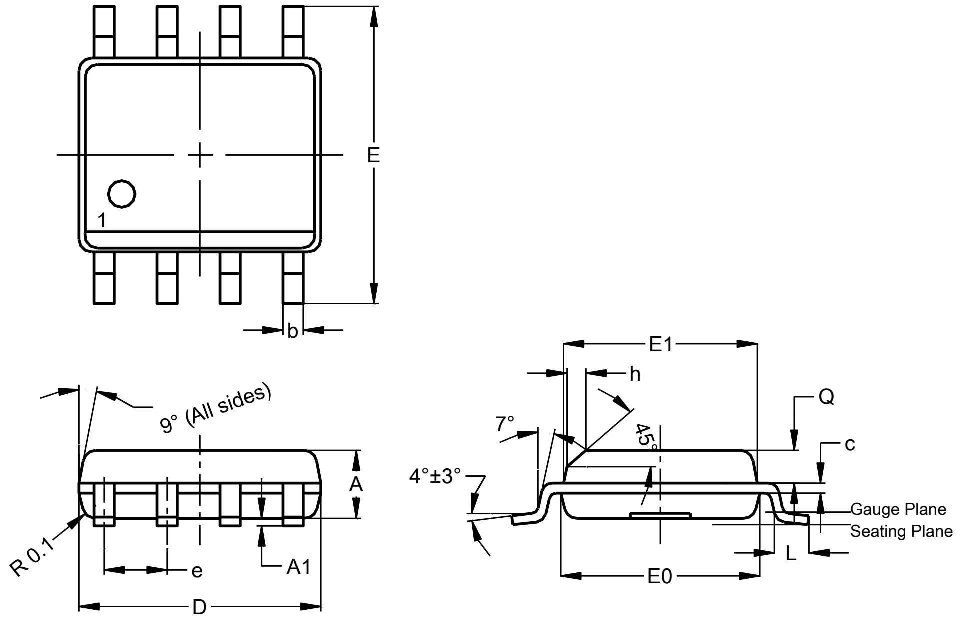
Gate Current vs Capacitive Load



Supply Current vs Frequency

Package Outline Dimensions

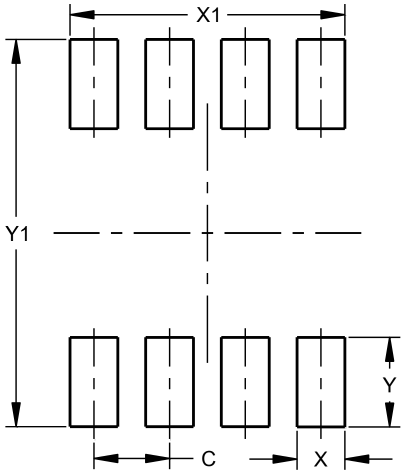
SO-8



SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50